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				Filing Date	Concurrently Herewith
				First Named Inventor	Katherine L. Saenger et al.
				Art Unit	NIA 2812
				Examiner Name	Not Yet Assigned GFEYER
Sheet	1	of	1	Attorney Docket Number	YOR920030530US1 CBLH/20140-00316-US

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NON PATENT LITERATURE DOCUMENTS				
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SBC	CA	JAKUB KEDZIERSKI, et al., Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation, IBM Semiconductor Research and Development Center pgs. 247-250		T ²
SBC	CB	B. GUILLAUMOT, et al., 75nm Damascene Metal Gate and High-k Integration for Advanced CMOS Devices, Cedex France, Meylan France, Marseille France, pgs. 355-358		
SBC	CC	KATHERINE L. SAENGER, et al., A Selective Etching Process for Chemically Inert High-k Oxides, Mat. Res. Soc. Symp. Proc. Vol. 745© 2003 Material Research Society, IBM Research Division, T.J. Watson Research Center		
SBC	CD	MATSUO J. YAMADA, , et al., Surface processing by gas cluster ion beams at the atomic (molecular) level, Ion Beam Engineering Experimental Laboratory, Kyoto University, Sakyo, Kyoto 606, Japan		

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